FORM PTO-1390 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE
(REV 11-98)

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER	
362-43 PCT/US	
U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR	
09/600931	
INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE
PCT/JP99/00225	22 January 1999
PRIORITY DATE CLAIMED	
23 January 1998	

TITLE OF INVENTION
DAMASCENE INTERCONNECTION AND SEMICONDUCTOR DEVICE

APPLICANT(S) FOR DO/EO/US
Yamamoto, et al.

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c) (2))
   a. ☒ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. ☒ A copy of the International Search Report (PCT/ISA/210).
8. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
9. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
10. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).
11. ☒ A copy of the International Preliminary Examination Report (PCT/IPEA/409).
12. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).

Items 13 to 20 below concern document(s) or information included:

13. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
14. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
15. ☒ A **FIRST** preliminary amendment.
16. ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
17. ☐ A substitute specification.
18. ☐ A change of power of attorney and/or address letter.
19. ☒ Certificate of Mailing by Express Mail
20. ☐ Other items or information:

Return-receipt postcard.
Copy of International Publication No. WO99/38204

534 Rec'd PCT/PTC 21 JUL 2000

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
09/600931	PCT/JP99/00225	362-43 PCT/US

21. The following fees are submitted:.

BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :

		CALCULATIONS PTO USE ONLY
☐	Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2) paid to USPTO and International Search Report not prepared by the EPO or JPO	**$970.00**
☒	International preliminary examination fee (37 CFR 1.482) not paid to USPTO but Internation Search Report prepared by the EPO or JPO	**$840.00**
☐	International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO	**$690.00**
☐	International preliminary examination fee paid to USPTO (37 CFR 1.482) but all claims did not satisfy provisions of PCT Article 33(1)-(4)	**$670.00**
☐	International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(1)-(4)	**$96.00**

ENTER APPROPRIATE BASIC FEE AMOUNT = **$840.00**

Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (e)). **$0.00**

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	
Total claims	14 - 20 =	0	x $18.00	**$0.00**
Independent claims	2 - 3 =	0	x $78.00	**$0.00**
Multiple Dependent Claims **(check if applicable).**			☐	**$0.00**

TOTAL OF ABOVE CALCULATIONS = **$840.00**

Reduction of 1/2 for filing by small entity, if applicable. Verified Small Entity Statement must also be filed (Note 37 CFR 1.9, 1.27, 1.28) **(check if applicable).** ☐ **$0.00**

SUBTOTAL = **$840.00**

Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (f)). + **$0.00**

TOTAL NATIONAL FEE = **$840.00**

Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) **(check if applicable).** ☒ **$40.00**

TOTAL FEES ENCLOSED = **$880.00**

Amount to be: refunded	$
charged	$

☒ A check in the amount of **$880.00** to cover the above fees is enclosed.

☐ Please charge my Deposit Account No. in the amount of to cover the above fees.
A duplicate copy of this sheet is enclosed.

☒ The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. **08-2461** A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

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SIGNATURE

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NAME

38,639
REGISTRATION NUMBER

21 July 2000
DATE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Yamamoto, et al.

Serial No.: Unassigned

Filed: Herewith

For: DAMASCENE INTERCONNECTION AND SEMICONDUCTOR DEVICE

Examiner: Unassigned

Group Art Unit: Unassigned

Docket: 362-43 PCT/US

Dated: July 21, 2000

Assistant Commissioner for Patents
Washington, DC 20231

PRELIMINARY AMENDMENT

Sir:

Prior to the examination of this application, please amend the application as follows:

IN THE CLAIMS:

Please amend the claims as follows:

Claim 7, line 1 thereof, delete "to 6".

Claim 14, line 1 thereof, change "any of claims 8 to 13 " to --claim 8--.

REMARKS

The amendment herein to the claims is made to delete the multiple dependency of Claims 7 and 14.

It is believed that the application is in proper form for examination and such action is respectfully solicited.

Respectfully submitted,

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SPECIFICATION

Damascene Interconnection and Semiconductor Device

TECHNICAL FIELD

This invention relates to damascene interconnections and semiconductor devices. More particularly, the invention relates to a damascene interconnection having a bonding pad formed by a pad trench and a metal or conductive film filling the pad trench, and to a semiconductor device using same.

PRIOR ART

Recently, so-called the damascene process has being adopted in providing multilevel interconnections for a semiconductor device having a metal or conductive film buried in the insulating film.

Briefly explaining a general damascene interconnection, an insulating film 2 formed on a semiconductor substrate 1 as shown in Figure 1(a) is etched using a mask of resist 3 patterned corresponding to an interconnection, as shown in Figure 1(b), thereby forming a trench 4. After removing away the resist 3, a conductive film 5 is formed covering the trench 4 as shown in Figure 1(c). Then, the conductive film 5 in areas other than the trench 4 is removed in a polishing process using, for example, a Chemical Mechanical Polish process (hereinafter referred to as "CMP process"), as shown in Figure 1(d).

It is known that, where removing the conductive film 5 by the CMP process, the greater is the opening area of the trench the higher is the polish rate on the conductive film buried in the trench, as shown in Figure 2. There encounters no especial problem in regions having a small trench opening area, such as in usual interconnections. However,

in regions having a large trench opening area, such as a bonding pad 6 shown in Figure 3, the conductive film 5 in the trench is polished into a dish-like form by an abrasive as shown in Figure 4, thus resulting in so-called dishing. Due to this, there are cases that disconnection or increase of resistance occurs in a central portion A where the wall thickness is reduced when providing connection between the bonding pad and the IC frame.

SUMMARY OF THE INVENTION

Therefore, it is a primary object of the present invention to provide a novel damascene interconnection and semiconductor device.

Another object of the invention is to provide a damascene interconnection capable of preventing resistance value increase or disconnection caused by dishing in a bonding pad, and a semiconductor device using the same.

A damascene interconnection according to the present invention, comprises: an interconnection trench formed in an insulating film and a pad trench communicating therewith; a protrusion formed by a portion not removed of the insulating film in the pad trench to decrease a substantial opening area of the pad trench; and a conductive film buried in the interconnection trench and the pad trench.

In the case of using such a damascene interconnection for a semiconductor device, such a semiconductor device, comprises: a semiconductor substrate; an insulating film formed on the semiconductor substrate; an interconnection trench formed on the insulating film and communicating with a semiconductor element; a pad trench formed on the insulating film and communicating with the interconnection trench; a protrusion formed by a portion of not removed of the insulating film in the pad trench and reducing a substantial opening area of the pad trench; and a conductive film buried in the

interconnection trench and the pad trench.

When removing the conductive film by a CMP process or the like, the protrusion dividing the pad trench serves as a stop of polishing by an abrasive. Consequently, so-called dishing will not occur that the conductive film in the pad trench is excessively removed. Thus, according to the invention, it is possible to prevent a bonding pad from being increased of resistance or causing disconnection resulting from dishing.

The protrusion may be formed not to divide the conductive film buried in the pad trench, or formed to divide the conductive film. However, where the conductive film is divided, another means is required to electrically couple together divided conductive film portions. The other means may be a contact hole for connecting between the conductive film formed in the insulating film and a conductive film arranged in a level lower than the insulating film. It should be noted that the contact hole is effective also where the conductive film in the pad trench is not divided by a protrusion.

The protrusion includes, in one embodiment, island protrusions distributed in a proper interval in the pad trench, and in another embodiment ridges.

The above described objects and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is an illustrative view showing a process for a general damascene interconnection;

Figure 2 is a graph showing a usual polish characteristic in CMP;

Figure 3 is an illustrative view showing a prior art;

Figure 4 is a sectional view on line IV-IV in Figure 3;

Figure 5 is an illustrative view showing one embodiment of the present invention;

Figure 6 is a sectional view on line VI-VI in Figure 5;

Figure 7 is an illustrative view showing a method for forming the Figure 5 embodiment;

Figure 8 is an illustrative view showing another embodiment of the invention;

Figure 9 is an illustrative view showing another embodiment of the invention;

Figure 10 is an illustrative view showing another embodiment of the invention;

Figure 11 is a sectional view on line - in Figure 10;

Figure 12 is an illustrative view showing another embodiment of the invention; and

Figure 13 is an illustrative view showing another embodiment of the invention.

BEST FORM FOR PRACTICING THE INVENTION

A semiconductor device 10 of this embodiment shown in Figure 5 and Figure 6 includes a semiconductor substrate 12 formed, for example, of silicon (Si) or the like. Note that the semiconductor substrate 12 may use any of other materials. Semiconductor elements, including active and/or passive elements, are formed on the semiconductor substrate 12, although they are not shown in the figure.

The semiconductor device 10 comprises a damascene interconnection 11 including, on the semiconductor substrate 12, an interconnection trench 16 extending from the semiconductor element (not shown) and a pad trench 18 connected to the interconnection trench 16. That is, an insulating film 14 is formed, for example, of silicon oxide (SiO_2) in a uniform film thickness on the semiconductor substrate. In the insulating film 14, the interconnection trench 16 and the pad trench 18 connected therewith are formed. The insulating film 14 may use any of other materials.

Note that Figure 5 and Figure 6 illustrate the insulating film 14 formed directly on the surface of the semiconductor substrate 12 in order for simplifying illustration and explanation. However, in the actual semiconductor device, one or a plurality of semiconductor element layers are formed on the semiconductor substrate 12 as well known in the art and an interconnection layers is formed as required on each of such semiconductor element layers. The interconnection trench 16 provides electrical connection between the semiconductor element (not shown) and the pad trench 18. The pad trench 18 serves as a bonding pad on which wire-bonding is to be made to a not-shown IC leadframe. That is, the pad trench 18 is a connection terminal to provide electric conduction of the semiconductor element on each layer to and from the IC leadframe.

It has been a conventional practice to form such a damascene interconnection 11 by merely filling a conductive film, such as of copper (Cu), aluminum (Al) or tungsten (W), in the interconnection trench 16 and pad trench 18.

In this embodiment, however, the following devising is implemented on the pad trench 18 comparatively large in opening area, in order to prevent against dishing as stated before. That is, the pad trench 18 has an insulating film 14 formed to be left as an island-spotted form. Consequently, the pad trench 18 is divided into unitary portions by island protrusions 20. However, the island protrusions 20 do not separate one portion from another portion of the pad trench 18, i.e. the pad trench 18 is continuous in areas except for the island protrusions 20. That is, the pad trench 18 in this embodiment has a large opening size but is reduced in substantial opening area by the presence of the island protrusions 20. Specifically, in this embodiment the pad trench 18 has a side determined as approximately 50 - 200 μm and an interval of the protrusions 20 determined as approximately 5 - 20 μm.

In the pad trench 18 thus having the island-spotted protrusions 20, a conductive film 22 is formed using a metal as mentioned before or conductive material in a manner similar to that of the interconnection trench 16. Thus, the semiconductor element (not shown) on the semiconductor device 10 is electrically coupled through the conductive film 22 buried in the interconnection trench 16 to the pad trench 18, i.e. the conductive film 22 buried in the pad trench 18. Due to this, by bonding a wire (not shown) to the conductive film 22 formed in the pad trench 18, the semiconductor element is put in electrical connection to the wire, i.e. to the IC leadframe.

Hereunder, explanation is made on a method to concretely manufacture a semiconductor device 10 of the embodiment having a damascene interconnection 11 as described above, with reference to Figure 7. Incidentally, in Figure 7 an insulating film 14 is formed directly on a surface of a semiconductor substrate 12. It should however be noted that the semiconductor device 10 in practical has a proper number of semiconductor element layers as stated before and Figure 7 depicts an interconnection structure having only one layer for the sake of convenience.

An insulating layer 14 is formed on a semiconductor substrate 12 by thermal oxidation process or the like, as shown in Fig. 7(a). Thereafter, the insulating film 14 is masked with patterned resist 24 to leave island protrusions 20. Etching is made to form an interconnection trench 16 and a pad trench 18. At this time, a plurality of island protrusions 20 are formed in the pad trench 18. After removing the resist 24, a conductive film 22 is formed over an entire surface of the semiconductor substrate 12 including the interconnection trench 16 and pad trench 18 by a CVD or hot sputter process, as shown in Fig. 7(c). Then, the conductive film 22 on the insulating film 14 is removed as shown in Fig. 7(d) by a CMP process.

In the CMP process, the semiconductor substrate 12 (including the insulating film

14 and the conductive film 22) is urged onto a polishing pad mounted on a polisher table. The table and the substrate holder are relatively rotated while supplying to the polishing pad a slurry containing abrasive particles. When the conductive film 22 on the insulating film 14 is removed, the polishing operation is finished. In this case, the abrasive particle for polishing is selected of kind (material, particle size, etc.) such that in CMP a polish rate on the insulating film 14 is lower than a polish rate on the conductive film 22. According to an experiment conducted by the present inventors, the polish rate in concrete is desirably given as (polish rate on the conductive film 22) / (polish rate on the insulating film 14) $\geqq$ 20 to 10. This is because in CMP the conductive film 22 on the insulating film 14 needs to be removed as rapid as possible. However, the insulating film 14 should be prevented from being damaged due to polishing, and the island projections 20 are to prevent over-polish to the conductive film 22 of the pad trench 18. Consequently, there is a necessity of providing the insulating film 14 with greater polish resistance than that of the conductive film 22.

According to this embodiment, in the process of removing the conductive film 22 (Figure 7(d)), the protrusions 20 (insulating film 14) having a low polish rate acts such that the conductive film 22 is decelerated in proceeding of polishing by the polish pad. Thus, the conductive film 22 in the pad trench 18 can be prevented from being removed to an excessive extent. This in turn makes it possible to prevent the pad trench 18 from increasing in resistance or occurrence of disconnection due to dishing.

That is, in the conventional art shown in Figure 3 and Figure 4, because the pad trench 6 is contacted in its entire opening by a polish pad (not shown), the pad trench 6 having a large opening area is partly over-polished into a result of dishing. On the contrary, in this embodiment, despite the pad trench entirely is large in opening area, the opening is divided into unitary portions wherein the opening area is small if considered

on a portion sandwiched between the island protrusions 20. Due to this, over-polish will not occur. As a result, a conductive film 22 in the pad trench 18 is given a planar surface as shown in Figure 6 and Figure 7(d).

In this manner, in the present invention, where using a CMP method having a polish characteristic that the polish rate increases with increase in opening area, the forming of protrusions in the pad trench reduces the substantial opening area thereby preventing dishing.

Incidentally, the protrusions 20 may be in a form to divide the pad trench 18 into portions. The shape of a protrusion may be a straight line as shown in Figure 8 or a squared-spiral form as shown in Figure 9.

That is, in the embodiment shown in Figure 8, a plurality of protrusions or ridges 20 are formed extending from respective outer edges of four sides of a rectangular pad trench 18. It should be noted that, in also this case, the other areas of the pad trench 18 are continuous with one another. In also this embodiment, the substantial opening area is reduced in the areas of between the protruding ridges 20, between protruding ridges extending from different sides and between the protruding ridge 20 and the inner edge of the pad trench 18.

In the embodiment of Figure 9, a pad trench 18 has one ridge 20 formed in a squared-spiral form. In the Figure 9 embodiment, because the ridge 20 is in the spiral form, the pad trench 18 is not divided into. In this manner, by forming the ridge 20 in the spiral form, the opening area is substantially reduced in the areas of between portions of the ridge 20 and between the ridge 20 and the pad trench 18 inner edge.

Meanwhile, if necessary, connection holes or contact holes 26 may be formed through a bottom of the pad trench 18 to provide electrical connection between the conductive film 22 and a not-shown lower-level conductive film through these contact

holes 26.

Explanation is made in detail on an embodiment having contact holes 26 formed through the insulating film 14, with reference to Figure 10 and Figure 11,. This embodiment is to be applied to a semiconductor device having another layer formed in a level lower the insulating film 14, as shown in Fig. 11. That is, another insulating film 28 is formed on a semiconductor substrate 12, and further another conductive film 30 is formed on the insulating film 28. The insulating film 14 is formed on the conductive film 30. In a bottom of the pad trench 18, a plurality of contact holes 26 are formed penetrating through the insulating film 14. When forming a metal or conductive film 22 in the pad trench 18, a metal or conductive material thereof is also filled in the contact holes 26 to provide electrical connection between the upper-leveled conductive film 22 and lower-leveled conductive film 30. By thus forming the contact holes 26 in the pad trench 18 and connecting between the conductive films 22 and 30, it is possible to eliminate the disadvantage as feared upon forming protrusions 20 in the pad trench 18.

That is, the protrusions or ridges if formed in the pad trench 18 results in volume decrease of the pad trench 18, i.e. volume reduction of the conductive film 22 of the pad trench 18. It is to be feared that the bonding pad be increased in electric resistance by volume reduction in the conductive film 22 of the pad trench 18. However, the conductive film 22 if coupled to the conductive film 30 as in the Figure 10 and Figure 11 embodiments increases the effective volume of the conductive film 22, thus properly suppressing the electric resistance from increasing.

In an embodiment shown in Figure 12, contact holes 26 are added to the structure of the Figure 8 embodiment to thereby make the conductive film 22 of the pad trench 18 integral with a lower-leveled conductive film.

In an embodiment of Figure 13, a ridge 20 is formed in a closed-loop form in a

manner different from the Figure 9 embodiment. Accordingly, in this embodiment the conductive film 22 of the pad trench 18 is divided into portions, in a manner different from the above embodiment. In this case, the contact holes 26 are especially effective. That is, the formation of contact holes 26 connects the conductive film 22 of the pad trench 18 to a lower-leveled conductive film 30 (Figure 11). Consequently, the divided portions of the conductive film 22 of the pad trench 18 are electrically coupled together through the conductive film 30. That is, in the Figure 13 embodiment, the ridge or protrusion 20 is formed in a closed-loop form. However, there encounters no problem with disconnection in the pad trench 18 due to the protrusion or ridge 20 because the conductive film 22 is coupled to the lower-leveled conductive film through the via holes 26.

Incidentally, in the present invention, the protrusion or ridge for reducing the actual opening area of the pad trench may be provided in plurality in the pad trench or employed one in number.

Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the present invention being limited only by the terms of the appended claims.

WHAT IS CLAIMED IS:

1. A damascene interconnection, comprising:

an interconnection trench formed in an insulating film and a pad trench communicating therewith;

a protrusion formed by a portion not removed of said insulating film in said pad trench to decrease a substantial opening area of said pad trench; and

a conductive film buried in said interconnection trench and said pad trench.

2. A damascene interconnection according to claim 1, wherein said protrusion is formed not to divide said conductive film buried in said pad trench.

3. A damascene interconnection according to claim 2, wherein said protrusion increase a plurality of island protrusions distributed at a proper interval in said pad trench.

4. A damascene interconnection according to claim 2, wherein said protrusion includes a ridge.

5. A damascene interconnection according to claim 1, wherein said protrusion is formed to divide said conductive film buried in said pad trench.

6. A damascene interconnection according to claim 5, wherein said protrusion includes a closed-loop ridge encompassing one part in said pad trench.

7. A damascene interconnection according to any of claims 1 to 6, further comprising a contact hole formed in said pad trench and electrically connecting between said conductive film and another conductive film arranged in a level lower than said insulating film.

8. A semiconductor device, comprising:

a semiconductor substrate;

an insulating film formed on said semiconductor substrate;

an interconnection trench formed on said insulating film and communicating with

a semiconductor element;

a pad trench formed on said insulating film and communicating with said interconnection trench;

a protrusion formed by a portion of not removed of said insulating film in said pad trench and reducing a substantial opening area of said pad trench; and

a conductive film buried in said interconnection trench and said pad trench.

9. A semiconductor device according to claim 9, wherein said protrusion is formed not to divide said conductive film buried in said pad trench.

10. A semiconductor device according to claim 9, wherein said protrusion includes a plurality of island protrusions distributed at a proper interval in said pad trench.

11. A semiconductor device according to claim 9, wherein said protrusion includes a ridge.

12. A semiconductor device according to claim 8, wherein said protrusion is formed to divide said conductive film buried in said pad trench.

13. A semiconductor device according to claim 12, wherein said protrusion includes a closed-loop ridge encompassing one portion in said pad trench.

14. A semiconductor device according to any of claims 8 to 13, further comprising another conductive film formed in a level lower than said insulating film, and a contact hole formed through said insulating film in said pad trench and electrically connecting between said conductive film and said other conductive film.

ABSTRACT OF THE DISCLOSURE

A semiconductor device includes an insulating film. On this insulating film, formed are an interconnection trench communicating with a semiconductor element and a pad trench communicating with the interconnection trench. In the pad trench, a protrusion is formed by leaving one part of the insulating film. A conductive film is formed over the insulating film including the interconnection and pad trenches. Thereafter, the conductive film is removed by a CMP process. At this time, the protrusion serves to prevent the conductive film in the pad trench from being over-polished.

FIG. 1

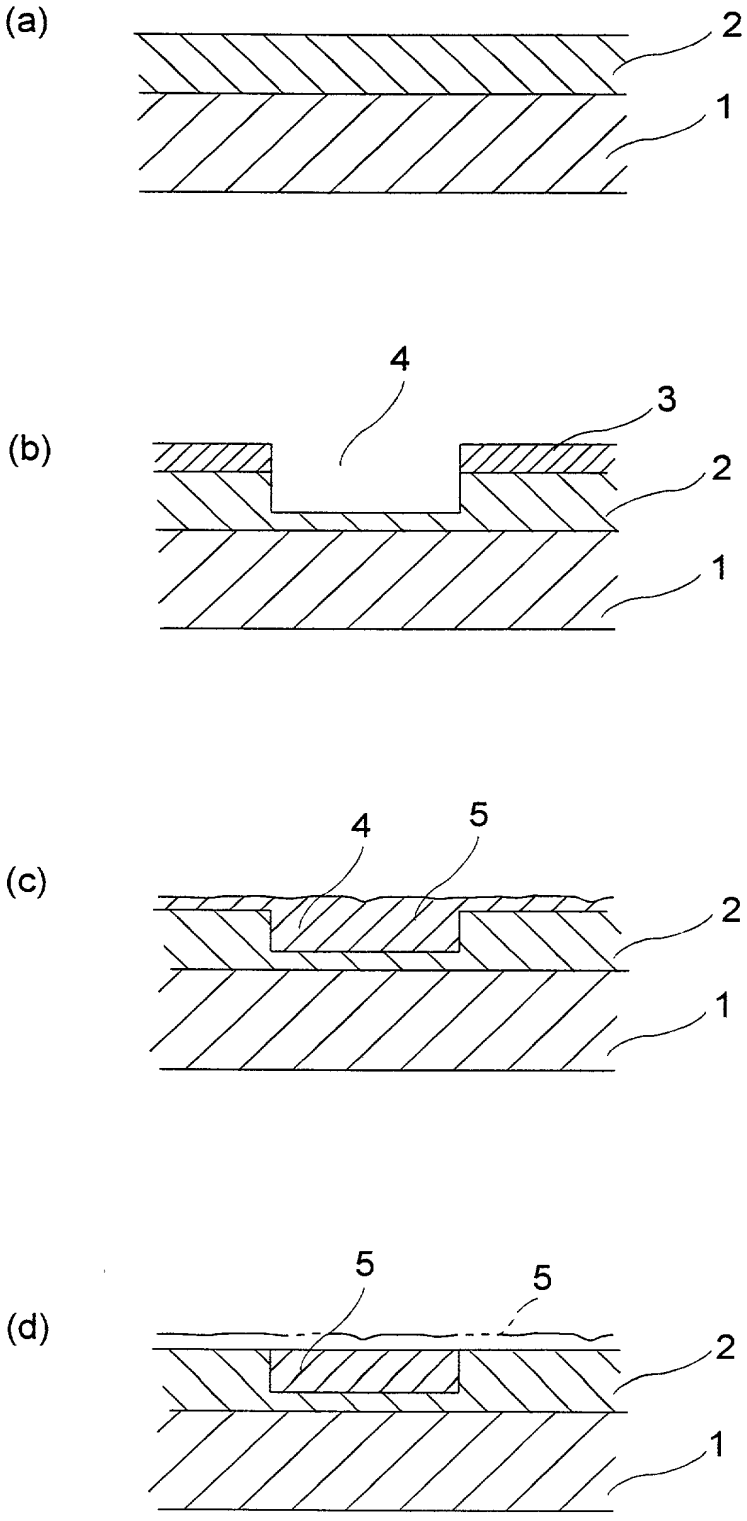
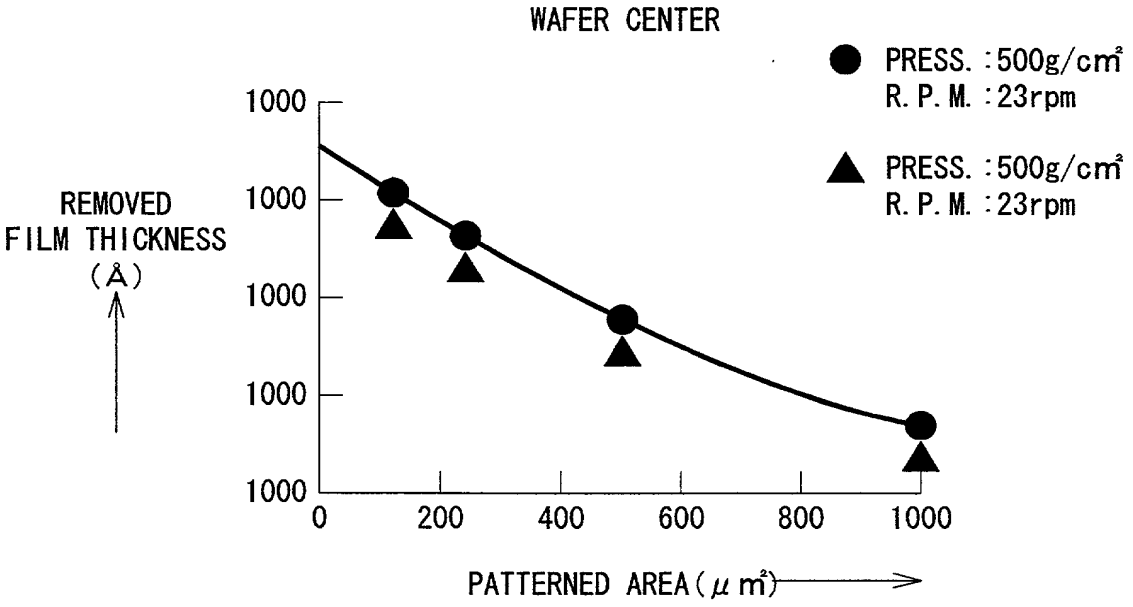


FIG. 2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PRESS. :500g/cm²
R. P. M. :23rpm
REMOVED
FILM THICKNESS
(Å)
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1000
1000
1000
0
200
400
600
800
1000
PATTERNED AREA (μm²)

FIG. 3

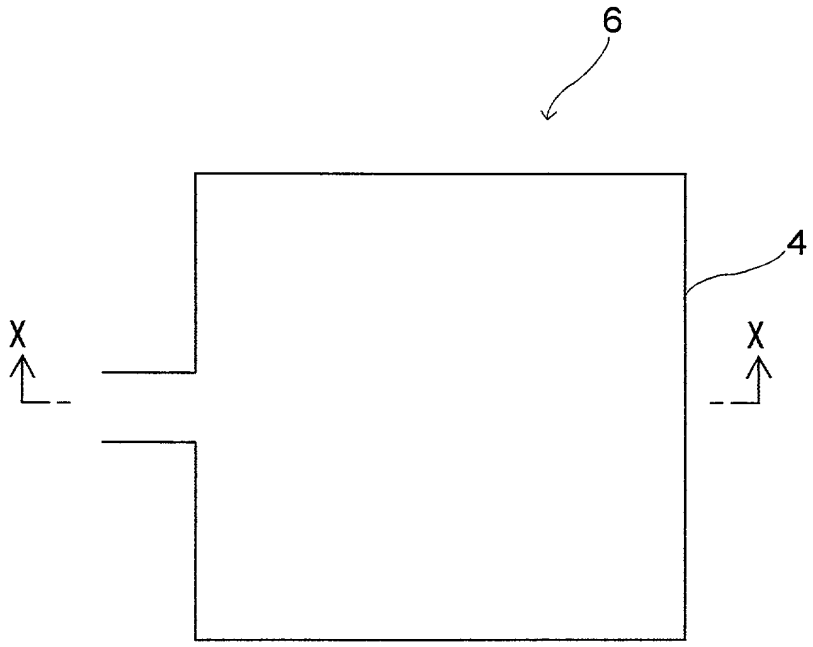

6
4
X
X

FIG. 4

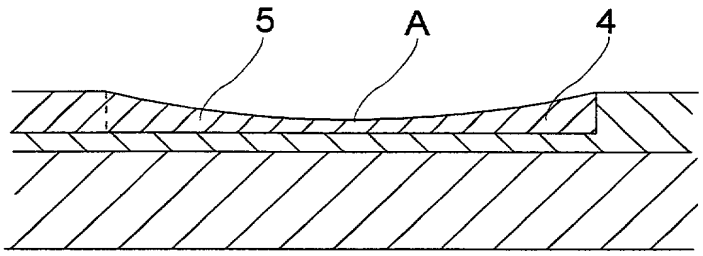


FIG. 5

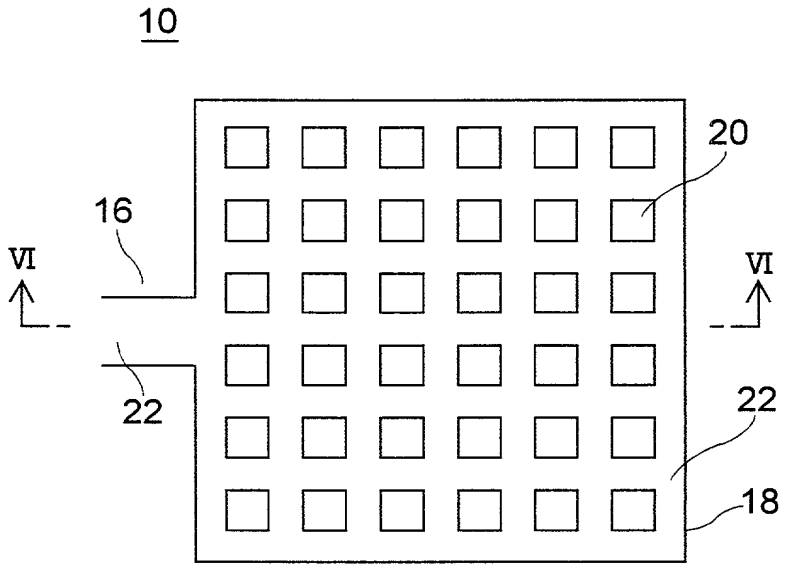


FIG. 6

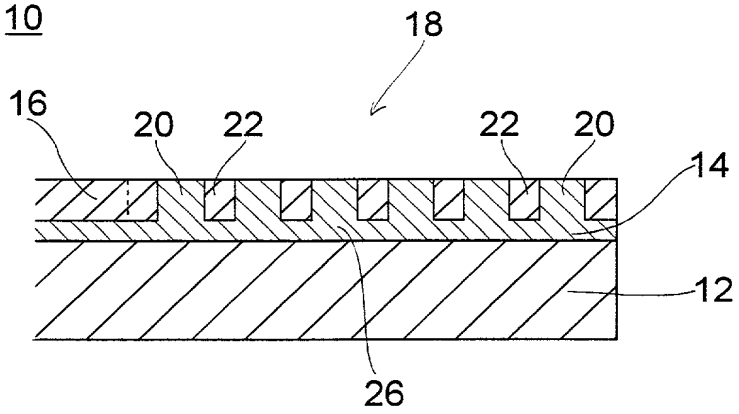


FIG. 7

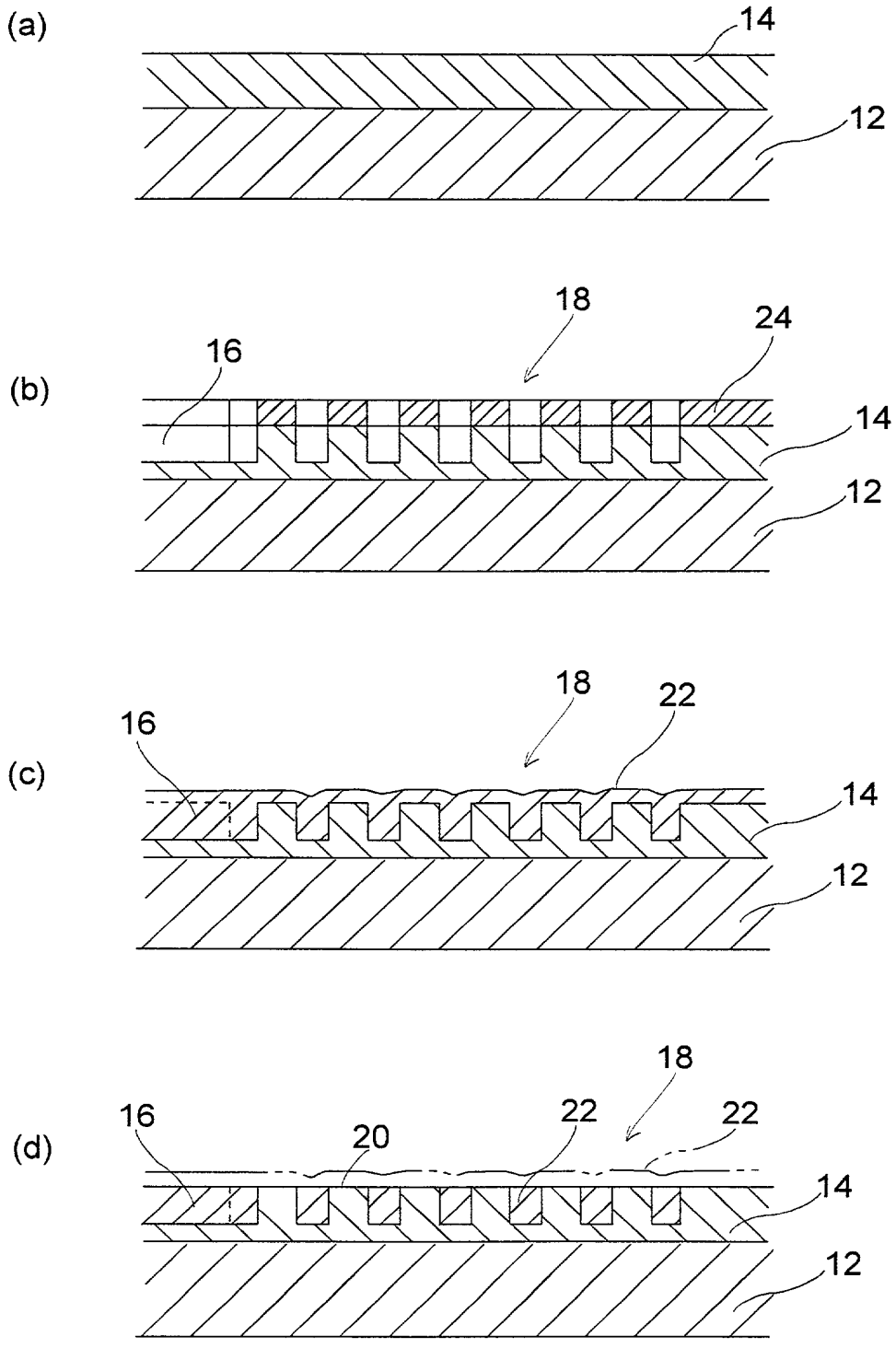


FIG. 8

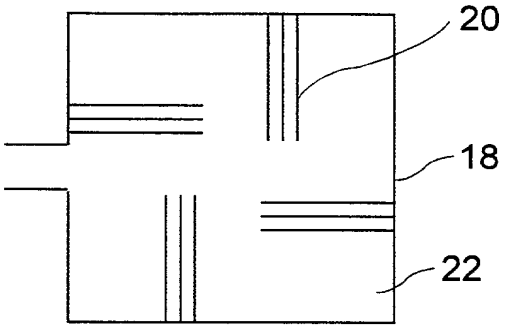


FIG. 9

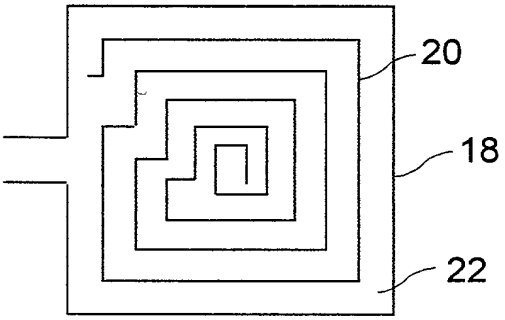


FIG. 10

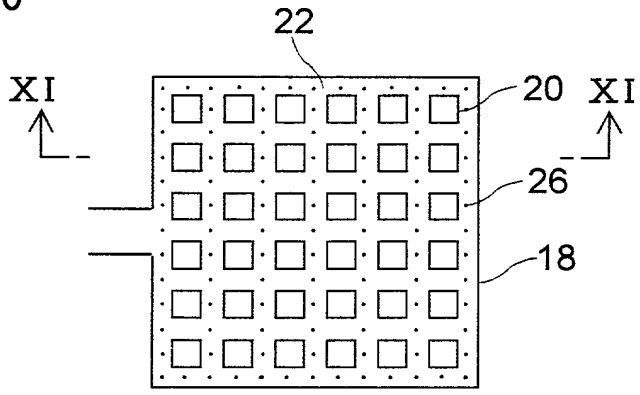


FIG. 11

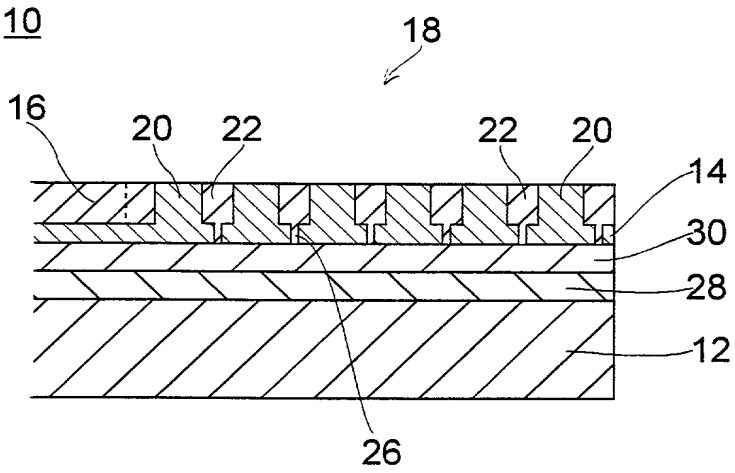


FIG. 12

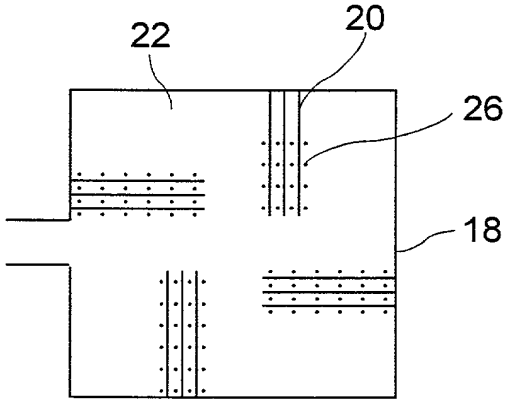
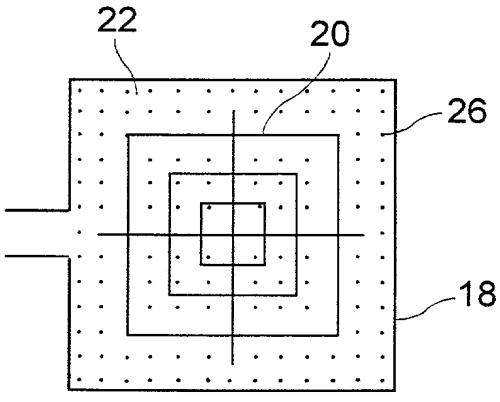


FIG. 13



PTO/SB/106 (8-96)
Approved for use through 9/30/98. OMB 0651-0032
Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

DAMASCENE INTERCONNECTION AND SEMICONDUCTOR DEVICE

上記発明の明細書（下記の欄でx印がついていない場合は、本書に添付）は、

the specification of which is attached hereto unless the following box is checked:

☐ __月__日に提出され、米国出願番号または特許協定条約国際出願番号を_____とし、
（該当する場合）_____ に訂正されました。

☒ was filed on January 22, 1999
as ~~United States Application Number~~ or
PCT International Application Number
PCT/JP99/00225 and was amended on
_____ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第３７編第１条５６項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

Japanese Language Declaration
(日本語宣言書)

私は、米国法典第３５編１１９条(a)-(d)項又は３６５条(b)項に基き下記の、米国以外の国の少なくとも一ヶ国を指定している特許協力条約３６５(a)項に基ずく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、印内をマークすることで、示しています。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s) 外国での先行出願			Priority Not Claimed 優先権主張なし
10-11354	Japan	23 January 1998	
(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	
(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	

私は、第３５編米国法典１１９条(e)項に基いて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No.) (出願番号)	(Filing Date) (出願日)

私は、下記の米国法典第３５編１２０条に基いて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約３６５条(c)に基ずく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第３５編１１２条第１項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第３７編１条５６項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)
(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

私は、私自身の知識に基ずいて本宣言書中で私が行なう表明が真実であり、かつ私の入手した情報と私の信じるところに基ずく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第１８編第１００１条に基ずき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行なえば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣言を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Japanese Language Declaration
(日本語宣言書)

委任状： 私に下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。（弁護士、または代理人の氏名及び登録番号を明記のこと）

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith *(list name and registration number)*

And I hereby appoint as principal attorneys:

書類送付先

The attorneys and agents of Hoffmann & Baron, LLP, as listed on the attachment (Page 5a)

直接電話連絡先： （名前及び電話番号）

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発明者の署名 日付	Inventor's signature Koji Yamamoto Date 18/July/2000
住所	Residence Ukyo-ku, Kyoto-shi, KYOTO 615-0045 Japan JPX
国籍	Citizenship Japanese
私書箱	Post Office Address c/o Rohm Co., Ltd. 21, Saiin Mizosaki-cho, Ukyo-ku, Kyoto-shi, KYOTO 615-0045 Japan
第二共同発明者名 200	Full name of second joint inventor, if any Nobuhisa KUMAMOTO
第二共同発明者の署名 日付	Second inventor's signature Date Nobuhisa Kumamoto 18/July/2000
住所	Residence Ukyo-ku, Kyoto-shi, KYOTO 615-0045 Japan JPX
国籍	Citizenship Japanese
私書箱	Post Office Address c/o Rohm Co., Ltd. 21, Saiin Mizosaki-cho, Ukyo-ku, Kyoto-shi, KYOTO 615-0045 Japan

（第三以降の共同発明者についても同様に記載し、署名をすること）

(Supply similar information and signature for third and subsequent joint inventors.)

第三共同発明者名		300 Full name of third joint inventor, if any Muneyuki MATSUMOTO	
第三共同発明者の署名	日付	Third inventor's signature Muneyuki Matsumoto	Date 18 / July / 2000
住所		Residence Ukyo-ku, Kyoto-shi, KYOTO 615-0045 Japan	
国籍		Citizenship Japanese	
私書箱		Post Office Address c/o Rohm Co., Ltd. 21, Saiin Mizosaki-cho, Ukyo-ku, Kyoto-shi, KYOTO 615-0045 Japan	
第四共同発明者名		Full name of fourth joint inventor, if any	
第四共同発明者の署名	日付	Fourth inventor's signature	Date
住所		Residence	
国籍		Citizenship	
私書箱		Post Office Address	
第五共同発明者名		Full name of fifth joint inventor, if any	
第五共同発明者の署名	日付	Fifth inventor's signature	Date
住所		Residence	
国籍		Citizenship	
私書箱		Post Office Address	
第六共同発明者名		Full name of sixth joint inventor, if any	
第六共同発明者の署名	日付	Sixth inventor's signature	Date
住所		Residence	
国籍		Citizenship	
私書箱		Post Office Address	

第七共同発明者名		Full name of seventh joint inventor, if any	
第七共同発明者の署名	日付	Seventh inventor's signature	Date
住所		Residence	
国籍		Citizenship	
私書箱		Post Office Address	
第八共同発明者名		Full name of eighth joint inventor, if any	
第八共同発明者の署名	日付	Eighth inventor's signature	Date
住所		Residence	
国籍		Citizenship	
私書箱		Post Office Address	
第九共同発明者名		Full name of ninth joint inventor, if any	
第九共同発明者の署名	日付	Ninth inventor's signature	Date
住所		Residence	
国籍		Citizenship	
私書箱		Post Office Address	
第十共同発明者名		Full name of tenth joint inventor, if any	
第十共同発明者の署名	日付	Tenth inventor's signature	Date
住所		Residence	
国籍		Citizenship	
私書箱		Post Office Address	

ATTACHMENT 5a

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